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<u>L20</u>	(711/131,132)[CCLS]	351	<u>L20</u>
<u>L19</u>	(711/131-173)![CCLS]	19017	<u>L19</u>
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<u>L17</u>	l13 and l2	88	<u>L17</u>
<u>L16</u>	l15 and l2	12	<u>L16</u>
<u>L15</u>	l14 and l2	12	<u>L15</u>
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<u>L12</u>	(macro\$1 or macroinstruction\$1) near3 (push\$4 or pop\$4)	171	<u>L12</u>
<u>L11</u>	(macro\$1 or macroinstruction\$1) near15 (push\$4 or pop\$4) near12 tempor\$5	0	<u>L11</u>
<u>L10</u>	L9 not 15	12	<u>L10</u>
<u>L9</u>	L8 near25 register\$1	16	<u>L9</u>
<u>L8</u>	(macro\$1 or macroinstruction\$1) near3 (push\$4 or pop\$4)	171	<u>L8</u>
<u>L7</u>	L6 not 15	1	<u>L7</u>
<u>L6</u>	(macro\$1 or macroinstruction\$1) near25 (push\$4 or pop\$4) near15 (mov\$3 or transfer\$4) near25 register\$1	8	<u>L6</u>
<u>L5</u>	(macro\$1 or macroinstruction\$1) near15 (push\$4 or pop\$4) near15 (mov\$3 or transfer\$4) near15 register\$1	7	<u>L5</u>
<u>L4</u>	(macro\$1 or macroinstruction\$1) near12 (push\$4 or pop\$4) near15 (mov\$3 or transfer\$4) near12 register\$1	7	<u>L4</u>
<u>L3</u>	(macro\$1 or macroinstruction\$1) near6 (push\$4 or pop\$4) near15 (mov\$3 or transfer\$4) near12 register\$1	7	<u>L3</u>
<u>L2</u>	(macro\$1 or macroinstruction\$1) near6 (push\$4 or pop\$4 or move)	918	<u>L2</u>
<u>L1</u>	(macro\$1 or macroinstruction\$1) near15 (push\$4 or pop\$4 or move)	1336	<u>L1</u>

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[E CLARKE](#)

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[PS] Realization of PRAMs: Processor Design - group of 5 »

J Keller, WJ Paul, D Scheerer - Proc. WDAG94, 8th Int. Workshop on Distributed Algorithms, ..., 1994 - [pv.fernuni-hagen.de](#)

... Push and pop instructions allow ... Therefore the register RAM's have to be either dual-ported or one has to use two single{ port RAM's and partition the ...

Cited by 21 - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [BL Direct](#)

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... should be able to handle tagged data items as single entities, with no ... Then we present the architecture's register structure and memory interface. ...

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JM Stichnoth, GY Lueh, M Cierniak - Proceedings of the ACM SIGPLAN 1999 conference on ..., 1999 - [portal.acm.org](#)

... bit to indicate whether it is a single instruction (and ... pointer, it is because of a push, pop, or call ... we must record the number of macro-instruction records ...

Cited by 35 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

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S Cho, S Park, S Kim, Y Kim, SW Jeong, BY Chung, ... - ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE ..., 2000 - [ieeexplore.ieee.org](#)

... pushq and popq are used to push or pop four registers in sequence ... In our first prototype

implementation, these datapath macro blocks were compiled, and all the ...

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A Language for Compositional Specification and Verification of Finite State Hardware Controllers - group of 4 »

EM CLARKE JR, DE LONG - [ieeexplore.ieee.org](#)

Page 1 PROCEEDINGS OF THE EEL. VOL. 79. NO, 9, SEPTEMBER 1991 t283 A Language for Compositional Specification and Verification of ...

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RISCs vs. CISCs for Prolog: a case study

G Borriello, AR Cherenson, PB Danzig, MN Nelson - ACM SIGPLAN Notices, 1987 - [portal.acm.org](#)

... ten SPUR local registers are used as temporaries by the macro-expansion code. ... better performance than the PLM for programs that push and pop choice points ...

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BK Holmer, B Sano, M Carlton, P Van Roy, AM ... - Journal of Logic Programming, 1996 - [info.ucl.ac.be](#)

... load and store of immediates, **single**-cycle double-word load and store, and **push** and **pop** **memory** operations. ... A double-word store or **push** is **single**-cycle (stdc ...
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A minimal CISC

DW Jones - ACM SIGARCH Computer Architecture News, 1988 - portal.acm.org
... **MACRO PUSHO** CODE DUP CODE DUP CODE SUB ENDMAC ... **PUSH** ptr ; ptr CODE
DUP ; ptr CODE
LOAD ; ptr PUSHO ; ptr ... CODE ONE ; ptr CODE SUB ; ptr CODE SUB ; ptr CODE **POP** ;
...

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TL Adams, RE Zimmerman - Proceedings of the third international conference on ..., 1989 -
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... 7) Microsoft@ Macro Assembler, Version 5.0. ... DOS execute child process function after
single-stepping had ... Data transfer includes move, **push**, **pop**, load effective ...
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Using a Java Optimized Processor in a Real World Application - group of 3 »
M Schoeberl - Proceedings of the First Workshop on Intelligent Solutions ... - jopdesign.com
... respect to stack manipulation in **pop** or **push**: **Pop** instructions reduce ... operand or
for stack spill on **push** instructions and ... a reset signal to a 32 **macro**-cell PLD ...
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IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

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Qing Wu; Qinru Qiu; Pedram, M.; Chih-Shun Ding;
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